

# ANIRBAN CHAKRABORTY, PH.D.

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## SUMMARY

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- 1.5 years experience in working as Resource Controller IP Engineer at Intel Corporation for the next generation of Server, Client, Networking and Graphics Roadmaps.
- Experienced Electrical Engineer with strong understanding of RTL Design, VLSI Simulation and Error Correction Coding.
- Knowledge on Physical Design, Place & Route, IR drop, Physical Verification (DRC/LVS).
- 5+ years of experience in System Designing using CAD tools like Synopsys Design Compiler, Synopsys PrimeTime, Synopsys VCS, Cadence Virtuoso, Cadence Innovus and Xilinx Vivado.
- 2+ years of experience in Electrical Engineering data analysis using Python and R.
- An excellent team player with an ability to quickly learn new techniques and work in a fast-paced environment.

## TECHNICAL SKILLS

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- **HDL Languages:** SystemVerilog, VHDL
- **Design Techniques:** Synthesis, Physical Design, Place & Route, IR drop, Physical Verification (DRC/LVS).
- **Developer and CAD Tools:** Cadence JasperGold, Synopsys Verdi, Synopsys Design Compiler, Synopsys PrimeTime, Synopsys VCS, Ansys PowerArtist, Cadence Virtuoso, Cadence Innovus, Xilinx Vivado, LTspice, PSpice, Electric Layout tool, Intel Quartus, ModelSim, MATLAB
- **Programming:** Python, R, C

## EXPERIENCE

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### IP Logic Design Engineer

[Intel Corporation](#)

June 2022 - Present  
Hillsboro, OR, U.S.A.

#### Resource Controller Development

- Implemented Registers for the Resource controller IP used in the next generation Intel SOCs.
- Implemented the logic of component activation and level determination in the Power Management logics used in the next generation Intel SOCs.
- Implemented Formal Verification Properties for the Power Management Logics used in Intel SOCs.
- Performed thorough analysis and implementation of the stimulus for accurate workload simulation of the next generation Intel SOCs.
- Implemented exhaustive clock gating throughout the Resource controller IP to obtain a Dynamic Clock Gating Efficiency (DCGE) of 95%.
- Implemented triggers for debug in the Resource controller IP used in the next generation Intel SOCs.
- Worked on group wide upgrade of Cheetah Tools like SpyGlass Lint, Siemens Calibre, etc.

### Graduate Research and Teaching

[University of North Texas](#)

Aug 2016 - May 2022  
Denton, TX, U.S.A.

#### RTL Design – *Technology used* - 45 nm and 28 nm CMOS Process in Synopsys

- 4+ years of experience in VHDL and SystemVerilog.
- Brainstormed and collaborated on Hardware Architecture Constraints.
- Automated RTL Design Verification using TCL and Testbench Scripts and performed Synthesis on Synopsys Design Compiler.
- Worked on FPGA and ASIC platform.
- Taught VHDL and mentored in Designing and Testing Digital circuits in ASICs and FPGAs

#### VLSI Design – *Technology used* - TSMC 180 nm CMOS Process in Cadence Virtuoso

- Investigated and verified the functionality of CMOS circuits.
- Performed Design, Testing and Simulation of Digital Circuits.
- Performed DRC check and Layouts of basic Digital Circuits

#### Error Correction Coding – Developing efficient Codes for Error Correction

- Experience in optimization of Codes.
- Investigated existing ECC and optimized their power and area requirement to improve the performance.
- Developed new and improved codes for NAND Flash architectures.

#### Data Analysis – Crowdsourced E-Gaming Framework for Untangled and Untangled III

- Conducted crowdsourcing event for Untangled and Untangled III to collect the data for investigating the problem of Application Mapping on Hardware.
- Converted the Mapped DFG into RTL Design using SystemVerilog and synthesized in ASIC platform.

#### Guest Faculty

Seacom Engineering College

July 2015 - Dec 2015  
Howrah, West Bengal, India

- Instructor for the Electrical Machines Course.

#### EDUCATION

**Ph.D., Electrical Engineering** – GPA – 3.812/4.00  
University of North Texas

Aug 2016 - May 2022  
Denton, TX, U.S.A.

- **Dissertation** – Novel Algorithms and Hardware Architectures for Computational Subsystems Used in Cryptography and Error Correction Coding.

#### M.E., Electrical Engineering

Indian Institute of Engineering Science and Technology, Shibpur – GPA – 4.00/4.00

July 2013 - April 2015  
Howrah, West Bengal, India

- **Thesis** – Performance Analysis of a Single Axis Controlled Repulsive type Magnetic Bearing.

**B.Tech., Electrical Engineering** – GPA – 8.63/10.00  
Techno India College of Technology

Aug 2009 - June 2013  
Kolkata, West Bengal, India

#### SCHOLARSHIPS, HONORS & NOMINATIONS

- **Tuition Benefit Program** – Toulouse Graduate School, UNT Aug 2016 - May 2022
- **IEEE HKN Lambda-Zeta Student Poster Competition** – Third Place April 2022
- **Scholars Day Poster Judge** – Honors College, UNT April 2022
- **Three times Outstanding TA Nominations** – Department of Electrical Engineering, UNT Aug 2019 - May 2022
- **Post Graduate Scholarship (GATE/GPAT)** – AICTE July 2013 - April 2015

#### PUBLICATIONS

##### Peer-Reviewed Journal Articles

- **A. Chakraborty**, Z. Simpson, R. D. Balavendran Joseph, and G. Mehta, “A Comparative Study of Gameplay of Different Sets of Players in an Engineering Mapping Game,” **International Journal of Computer and Information Technology**(2279-0764), vol. 10, no. 4. Asian Online Journals, Jul. 31, **2021**. doi: [10.24203/ijcit.v10i4.127](https://doi.org/10.24203/ijcit.v10i4.127).
- **A. Chakraborty**, E. Ojo, B. Quonoey, and G. Mehta, “Improving Learning Experience of People with Cognitive Disabilities Using Serious Games: A Review,” **European Scientific Journal ESJ**, vol. 17, no. 35. **European Scientific Institute, ESI**, Oct. 31, **2021**. doi: [10.19044/esj.2021.v17n35p1](https://doi.org/10.19044/esj.2021.v17n35p1).
- **A. Chakraborty**, Z. P. Simpson, J. Tunks, and G. Mehta, “Solving Electrical Engineering Puzzles Using Spatial Reasoning,” **Journal of Education and Culture Studies**, vol. 2, no. 3. Scholink Co, Ltd., p. 227, Aug. 29, **2018**. doi: [10.22158/jecs.v2n3p227](https://doi.org/10.22158/jecs.v2n3p227).

##### Conference Proceedings

- **A. Chakraborty**, M. Varanasi, O. N. Garcia, and G. Mehta, “Area and Power analysis of a Scalable Primitive Polynomial computation circuit over the field GF(2),” **2022 IEEE 15th Dallas Circuit And System Conference (DCAS)**. IEEE, Jun. 17, **2022**. doi: [10.1109/dcas53974.2022.9845656](https://doi.org/10.1109/dcas53974.2022.9845656).
- Z. Simpson, **A. Chakraborty**, M. Varanasi, G. Mehta, and O. N. Garcia, “Power, Performance, and Area Analysis of Hardware Design Techniques for GF(2k) Greatest Common Divisor computation,” **2022 IEEE 15th Dallas Circuit And System Conference (DCAS)**. IEEE, Jun. 17, **2022**. doi: [10.1109/dcas53974.2022.9845594](https://doi.org/10.1109/dcas53974.2022.9845594).
- **A. Chakraborty**, T. Santra, D. Roy, and S. Yamada, “Modelling and stability analysis of a repulsive type magnetic bearing,” **2015 International Conference on Energy, Power and Environment: Towards Sustainable Growth (ICEPE)**. IEEE, Jun. **2015**. doi: [10.1109/epetsg.2015.7510149](https://doi.org/10.1109/epetsg.2015.7510149).

## Book Chapters

- **A. Chakraborty**, "Evolution of the Internet of Things and Fundamentals of Human-Machine Interaction," **Human-Machine Interaction and IoT Applications for a Smarter World**. CRC Press, pp. 3–14, Jun. 13, 2022. doi: [10.1201/9781003268796-2](https://doi.org/10.1201/9781003268796-2)